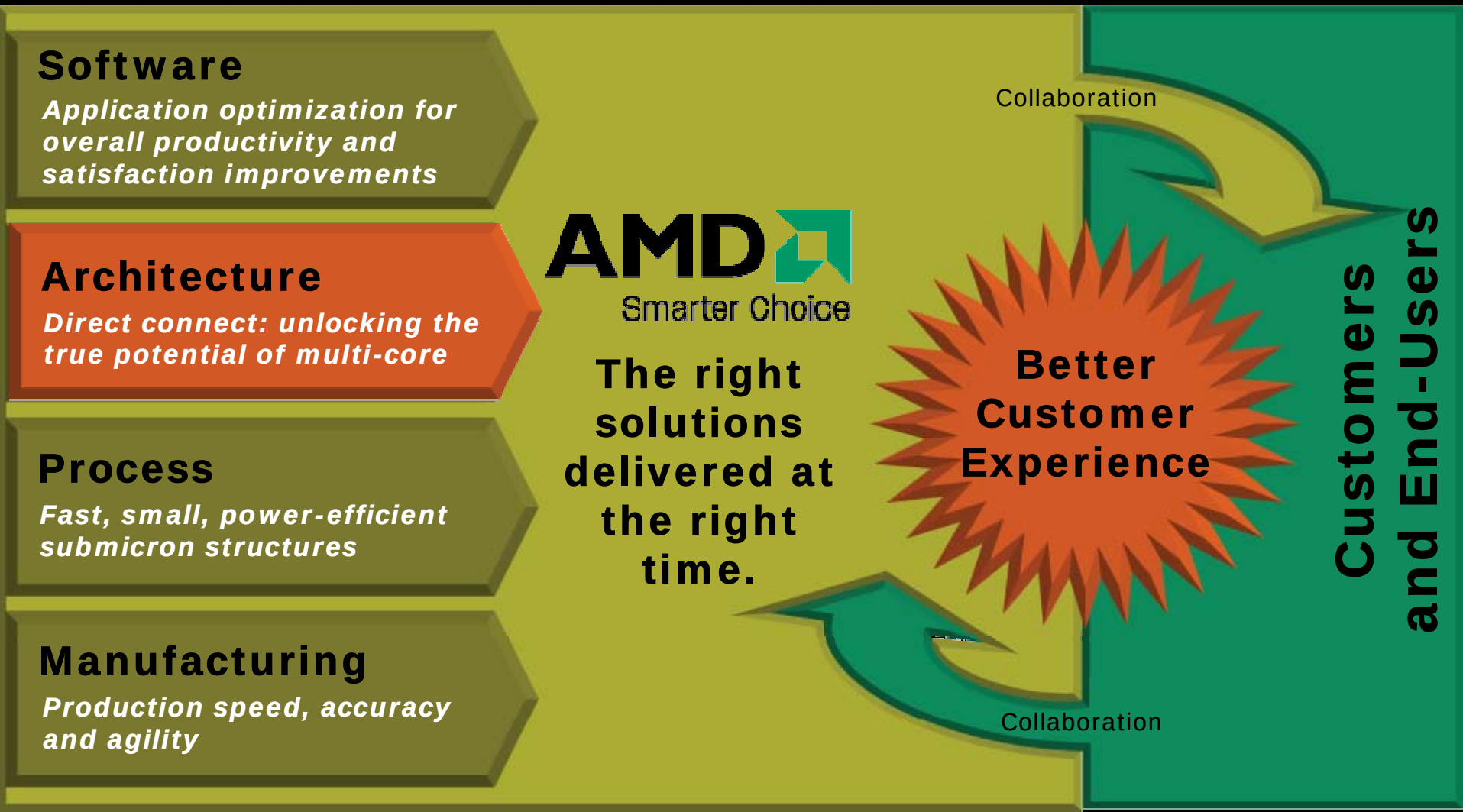
2006 Technology Analyst Day

Phil Hester
Senior Vice President and
Chief Technology Officer

June 1, 2006

Our Goal: Create the Best Customer Experience with the Highest Possible Value




Technology is Only
as Good as the
Experience it Creates

What Our Customers Are Telling Us

What Our Customers Are Telling Us

Server

Performance,
power efficiency, scalability

Improved reliability,
availability, serviceability

Need ability to
differentiate efficiently

Common architecture
top to bottom

What Our Customers Are Telling Us

Mobile

Choice of wireless and graphics

Validated reference designs – improved time to market

Better battery life

Low power processors

What Our Customers Are Telling Us

Desktop

Power efficiency

Continue driving the enthusiast market

Provide a commercially stable platform

Choice of validated chipsets

How that Translates into Our Design Priorities at the Chip and Platform Levels

Continued Performance and Power Efficiency Improvements

Balance of single thread vs. multiple thread performance

Enable high performance on diverse workloads

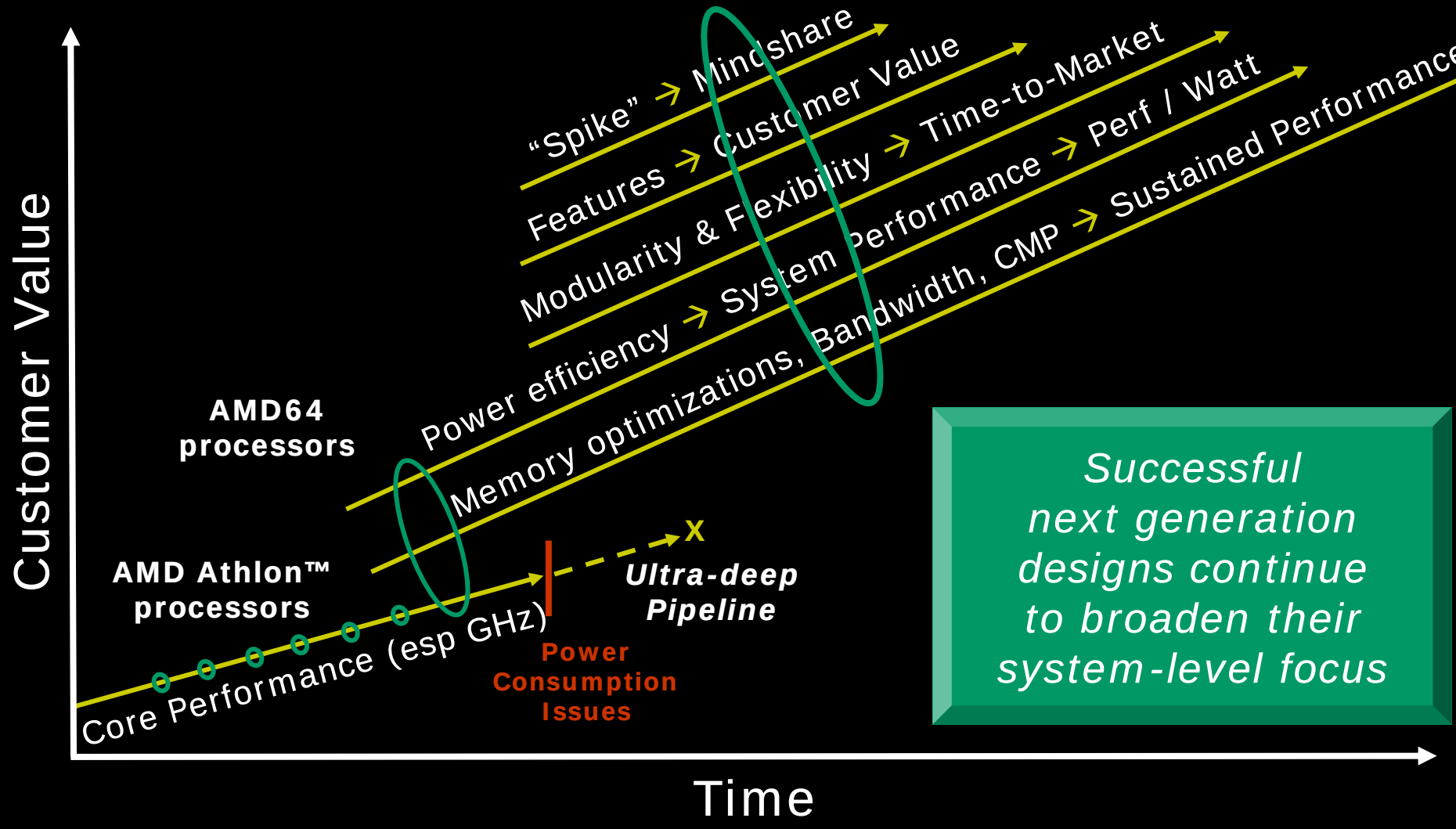
Easy/rapid tailoring of designs to market needs

The right technologies at the right time

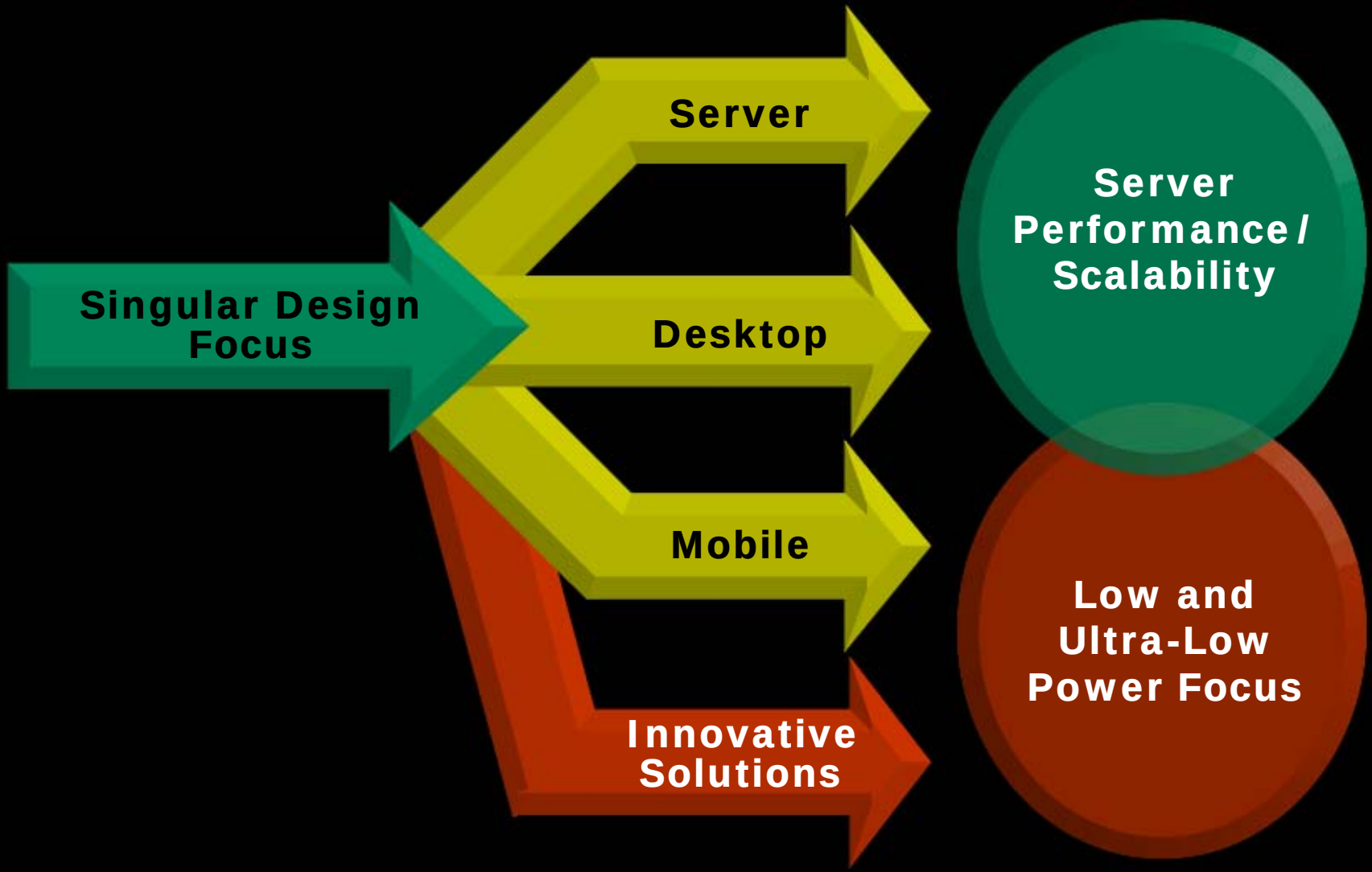
Parallel design efforts

Constant customer review of our directions

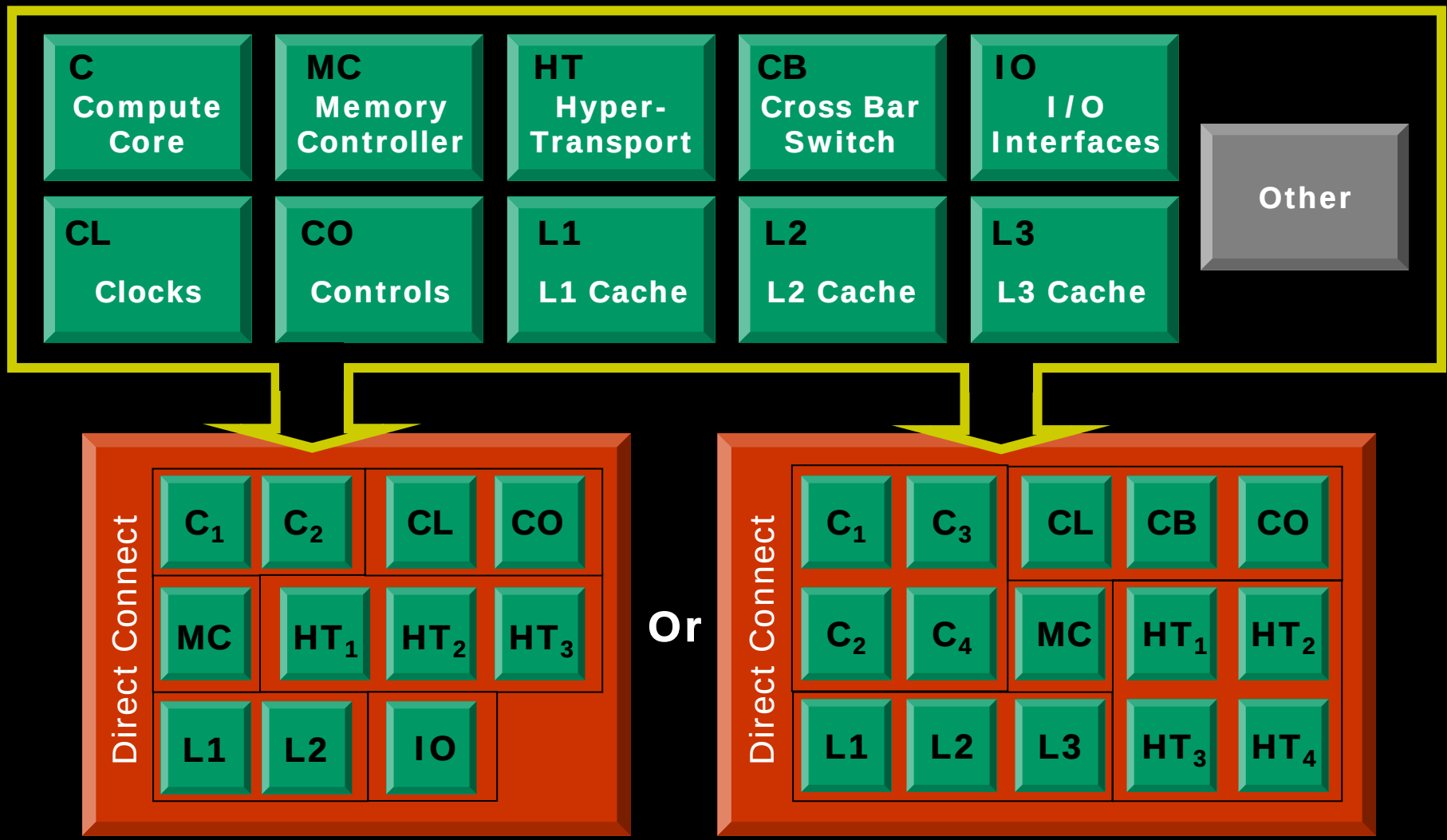
Customer Value Trends



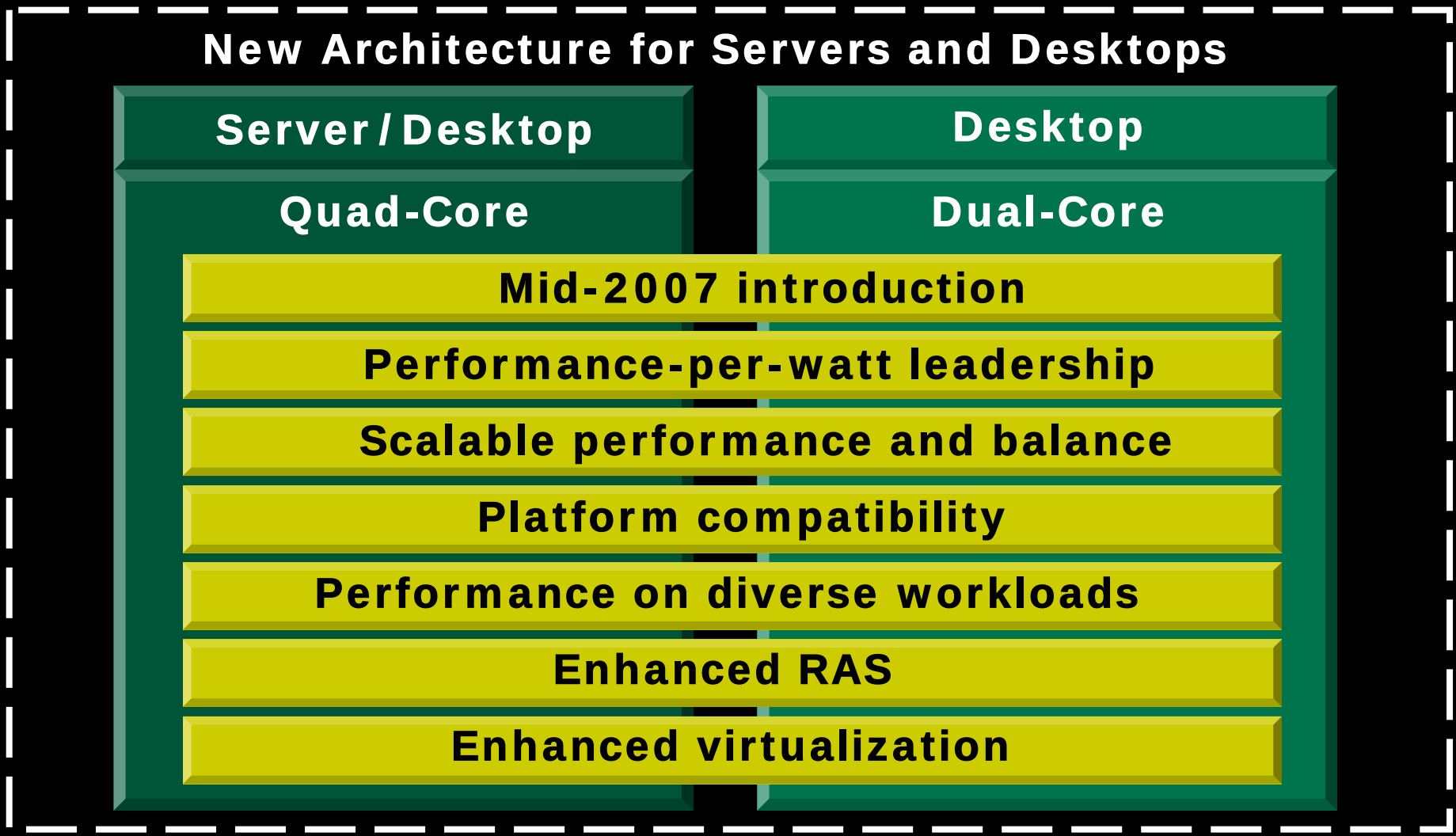
Diversifying Design Directions to Better Serve Customers and End-Users



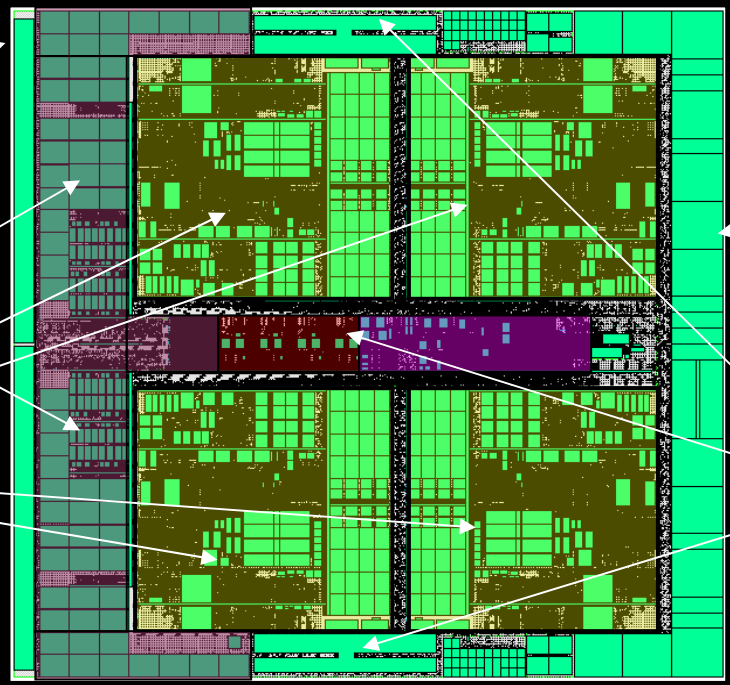
Modular Design Focus for Fast Development Cycles, Highly Tailored Solutions



Powering the Next Generation of AMD64 Leadership



A Closer Look at AMD's Next Generation Server and Desktop Architecture



True quad core die

Expandable shared L3 cache

IPC enhanced CPU cores

- 32B instruction fetch
- Enhanced branch prediction
- Out-of-order load execution
- Up to 4 DP FLOPS/cycle
- Dual 128-bit SSE dataflow
- Dual 128-bit loads per cycle
- Bit Manipulation extensions (LZCNT/POPCNT)
- SSE extensions (EXTRQ/INSERTQ, MOVNTSD/MOVNTSS)

Optimized for 65nm SOI and beyond

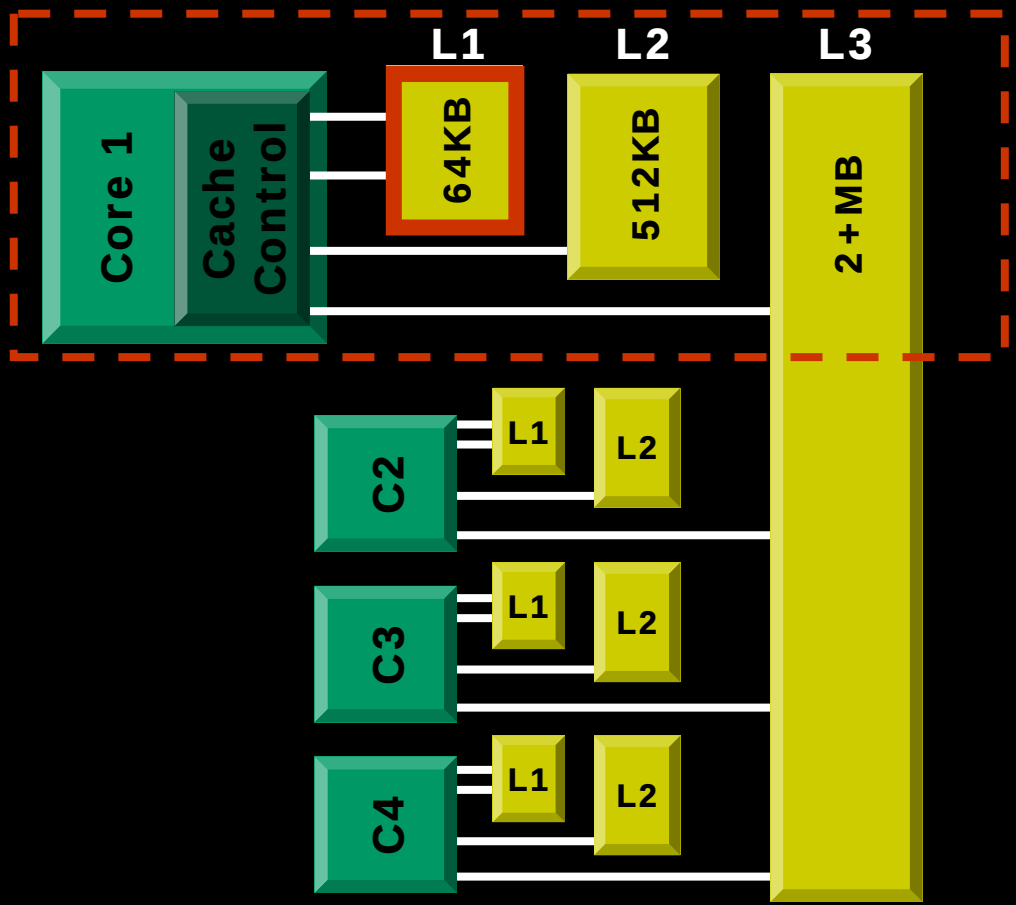
Enhanced Direct Connect Architecture and Northbridge

- HT-3 links (Up to 5.2GT/sec)
- Enhanced crossbar
- DDR2 with migration path to DDR3
- FBDIMM when appropriate
- Enhanced power management
- Enhanced RAS

AMD

Balanced, Highly Efficient Cache Structure

Superior memory handling reduces the need for "brute force" cache sizes

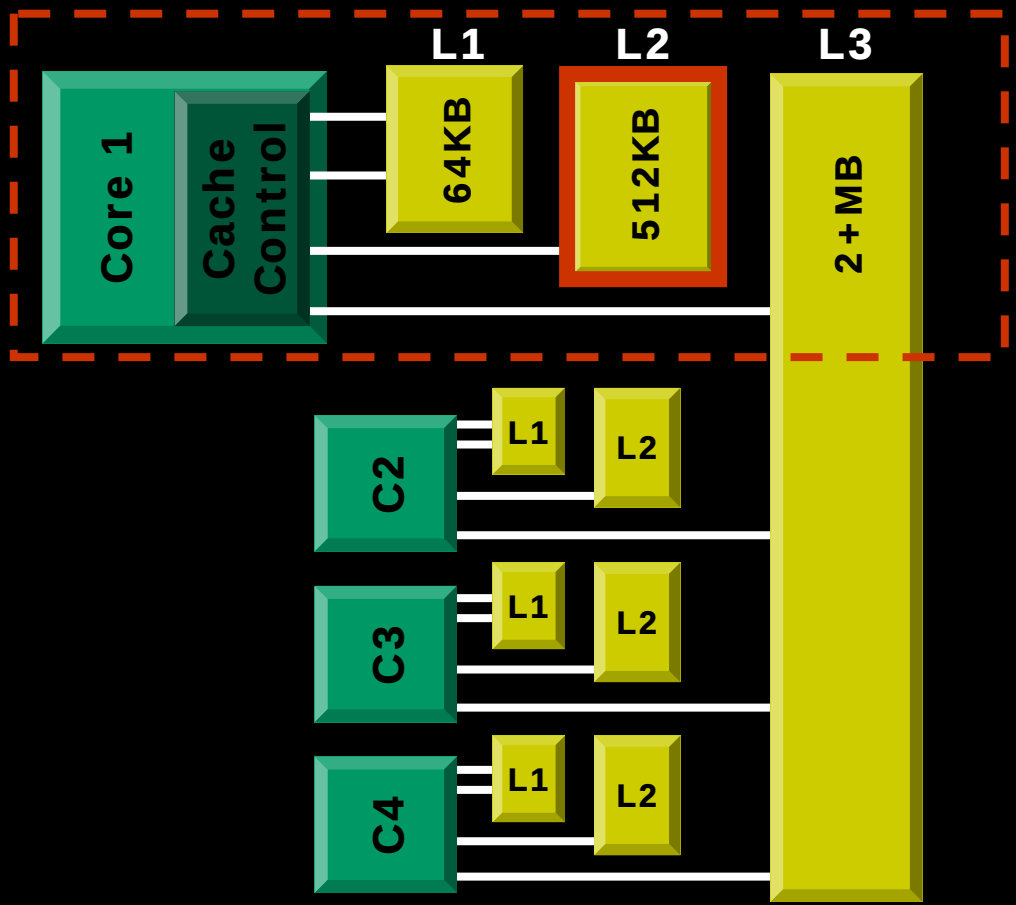


Dedicated L1

- Locality keeps most critical data in the L1 cache
- Lowest latency
- ~95% of hits
- 2 128 bit data paths
- 2 loads per cycle

Balanced, Highly Efficient Cache Structure

Superior memory handling reduces the need for "brute force" cache sizes

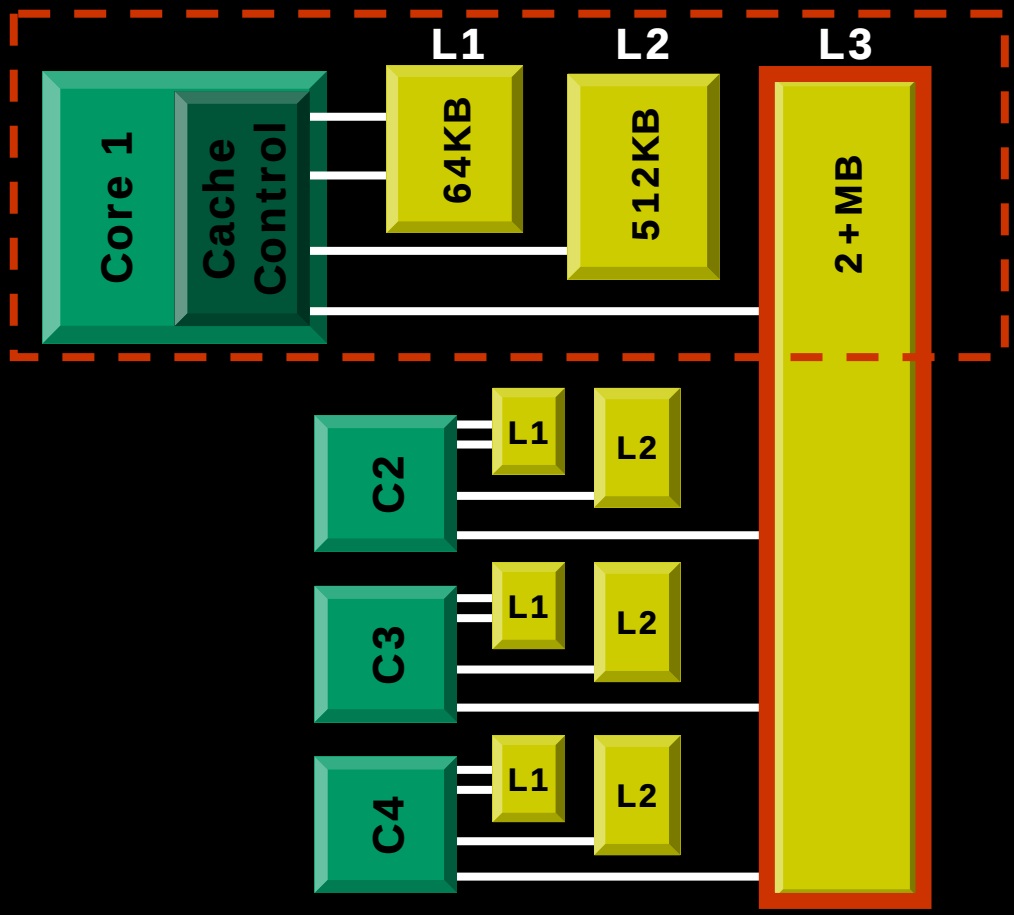


Dedicated L2

- Sized to accommodate the majority of working sets today
- Dedicated to eliminate conflicts common in shared caches

Balanced, Highly Efficient Cache Structure

Superior memory handling reduces the need for "brute force" cache sizes

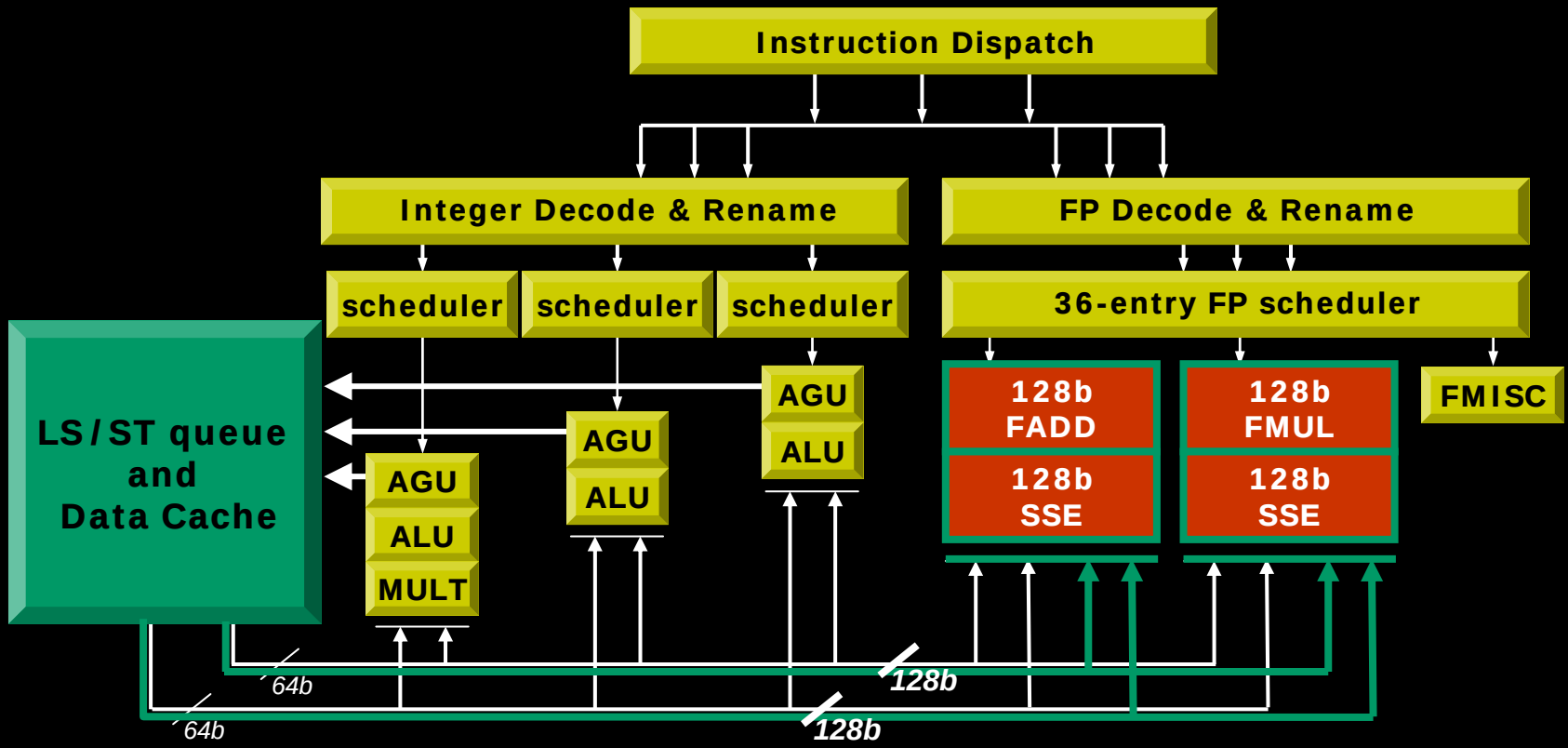


Shared L3 – *NEW*

- Optimized memory use and allocation for multi-core
- Highly efficient embedded memory controllers allow for appropriate size today
- Ready for expansion at the right time for customers

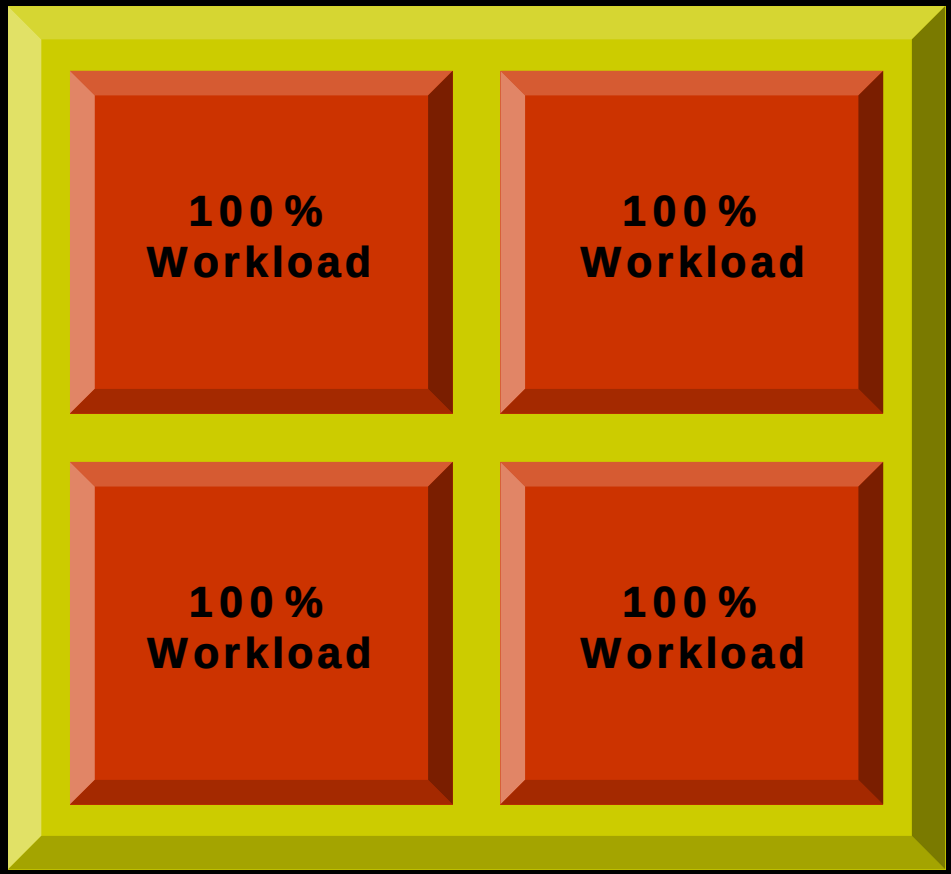
128-bit SSE and 128-bit Loads

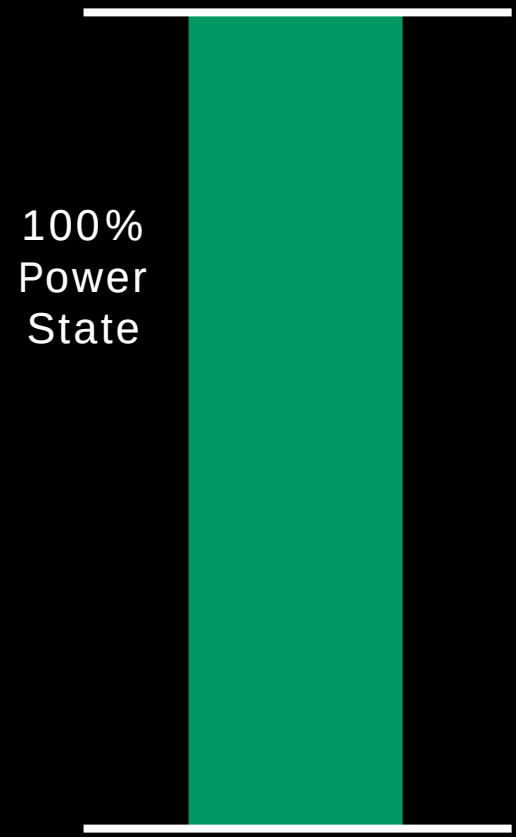
Comprehensive set of upgrades for improved performance on floating point- and graphics-intensive applications



DICE: Dynamic Independent Core Engagement

Ability to dynamically and individually adjust core frequencies for improved power efficiency





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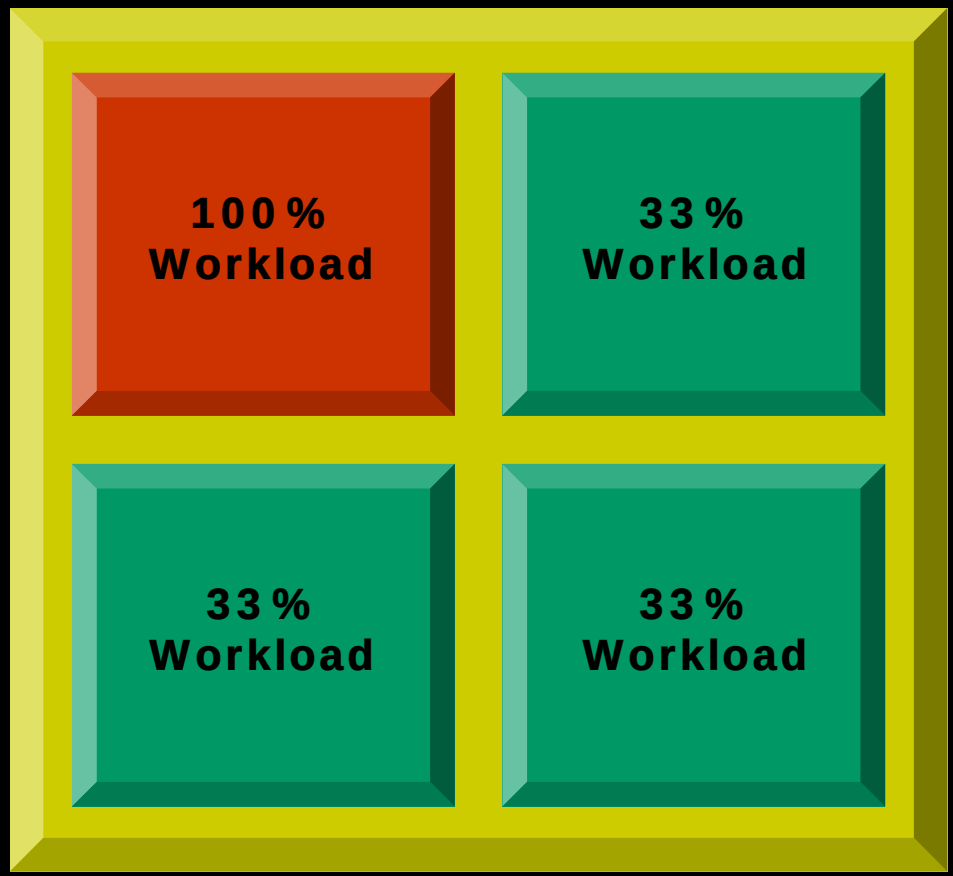

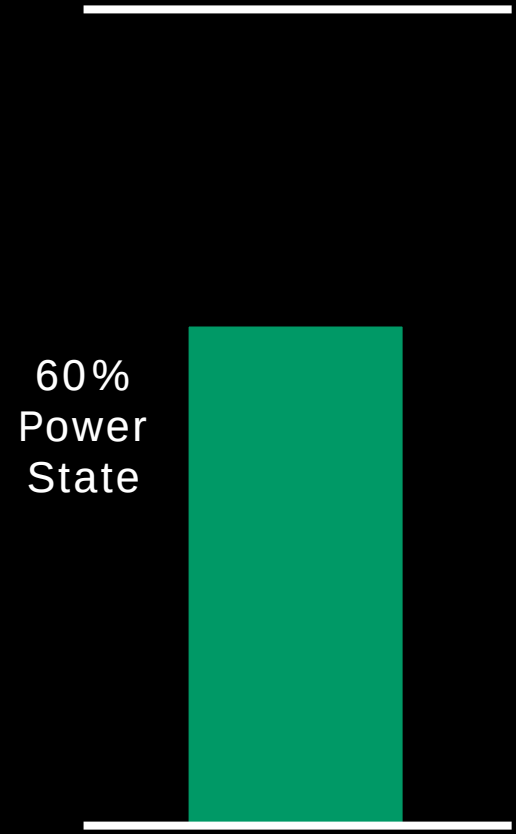

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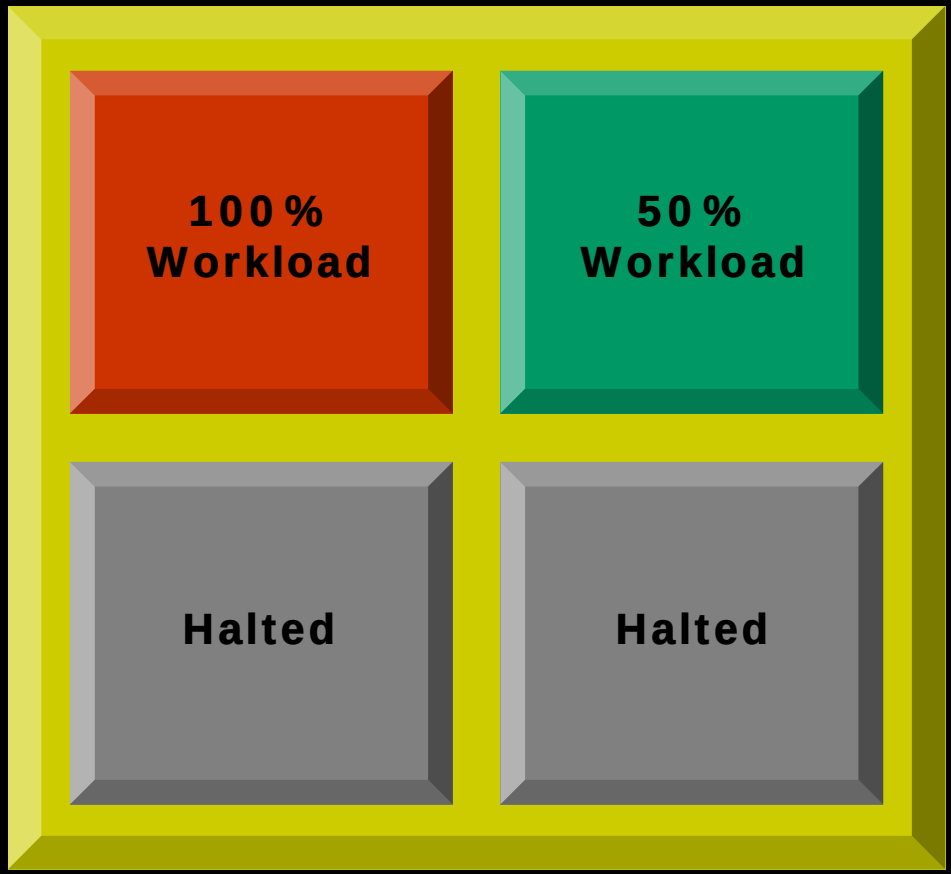
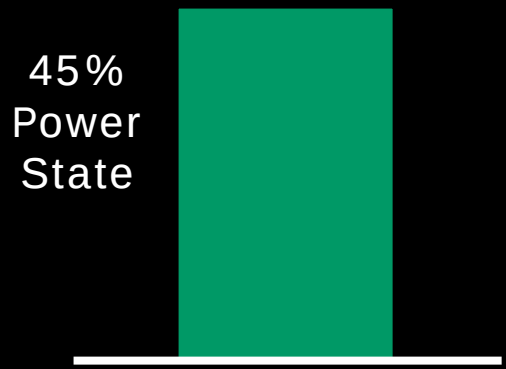
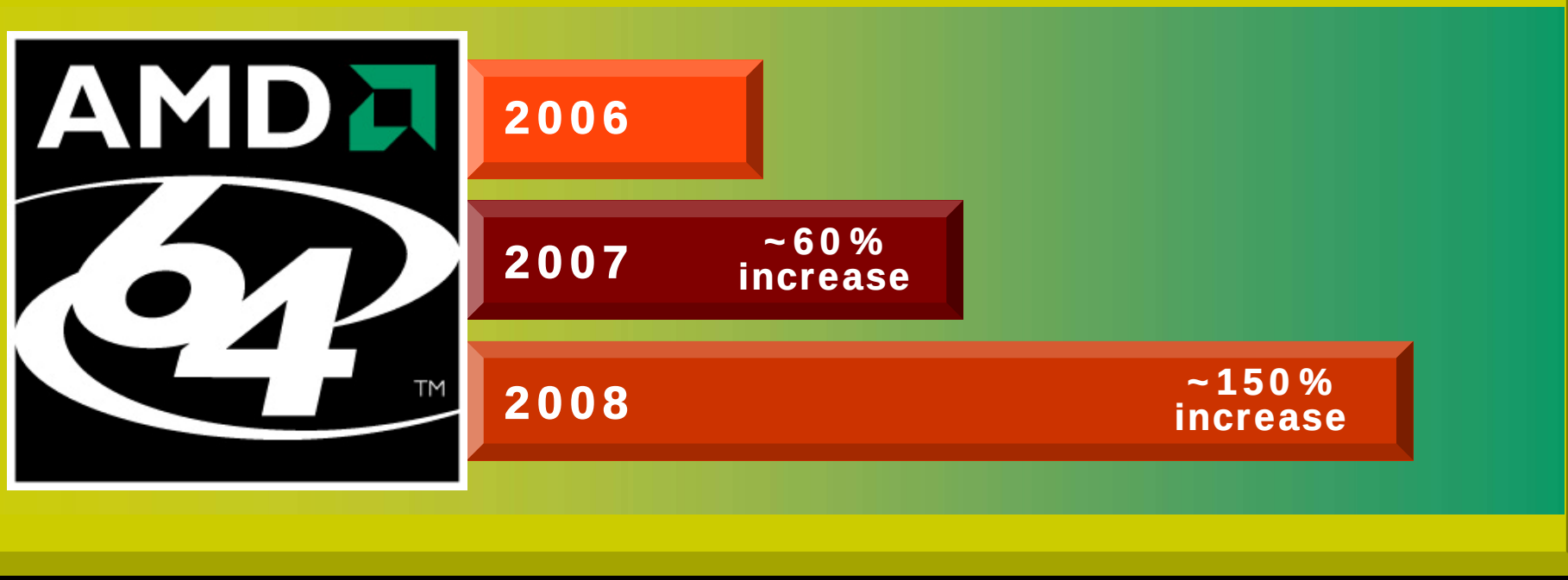




Continuing Leadership in Platform Performance and Power Efficiency

Performance-per-Watt

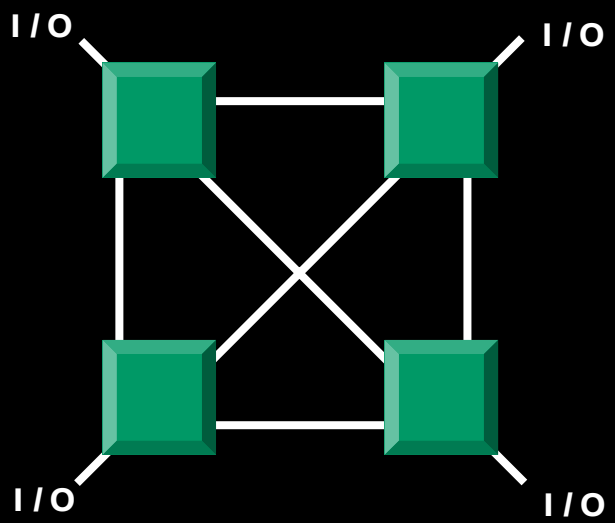


Performance projections based on modeling and a baseline of 2006 performance

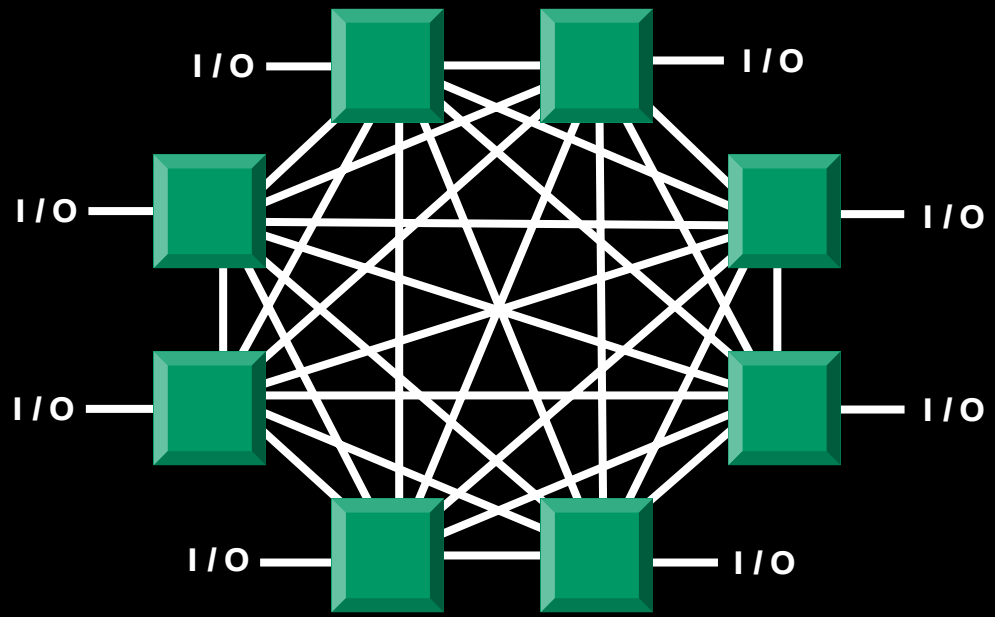
Source: AMD planned

Up to Four 16-bit HyperTransport™ Links, or Eight 8-bit Links

Increased number of higher bandwidth links for optimum multi-processor application performance



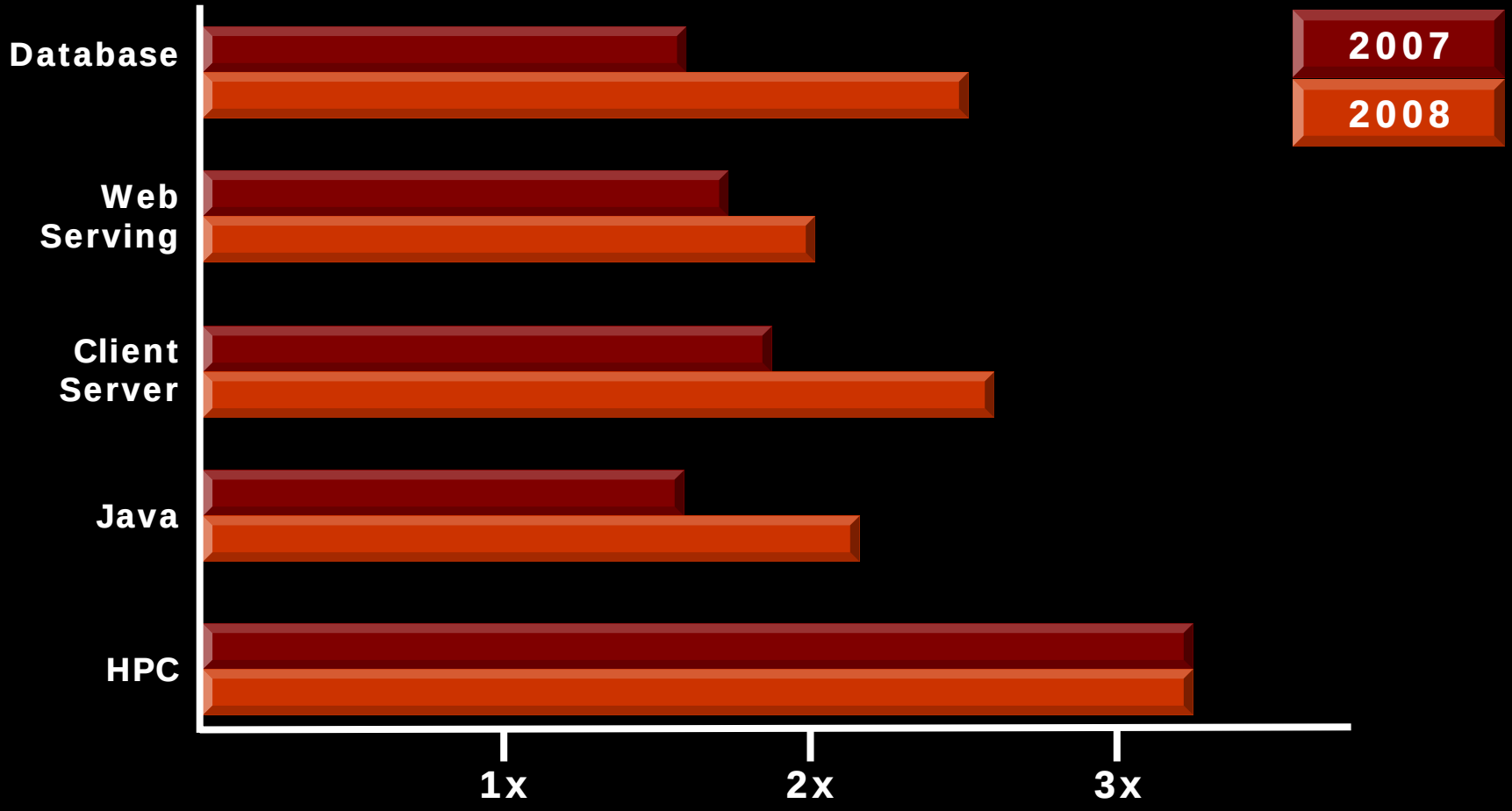
Fully connected
4-socket, 16 core server



Fully connected 8-socket, 32 core server with single memory hop

Enables both traditional and blade scale up systems

Critical Performance Increases Where it Matters Most for Enterprises



Performance projections based on modeling and a baseline of 2006 performance

Source: AMD planned

AMD

John Fowler

Executive Vice President

Sun Systems Group

Sun Microsystems

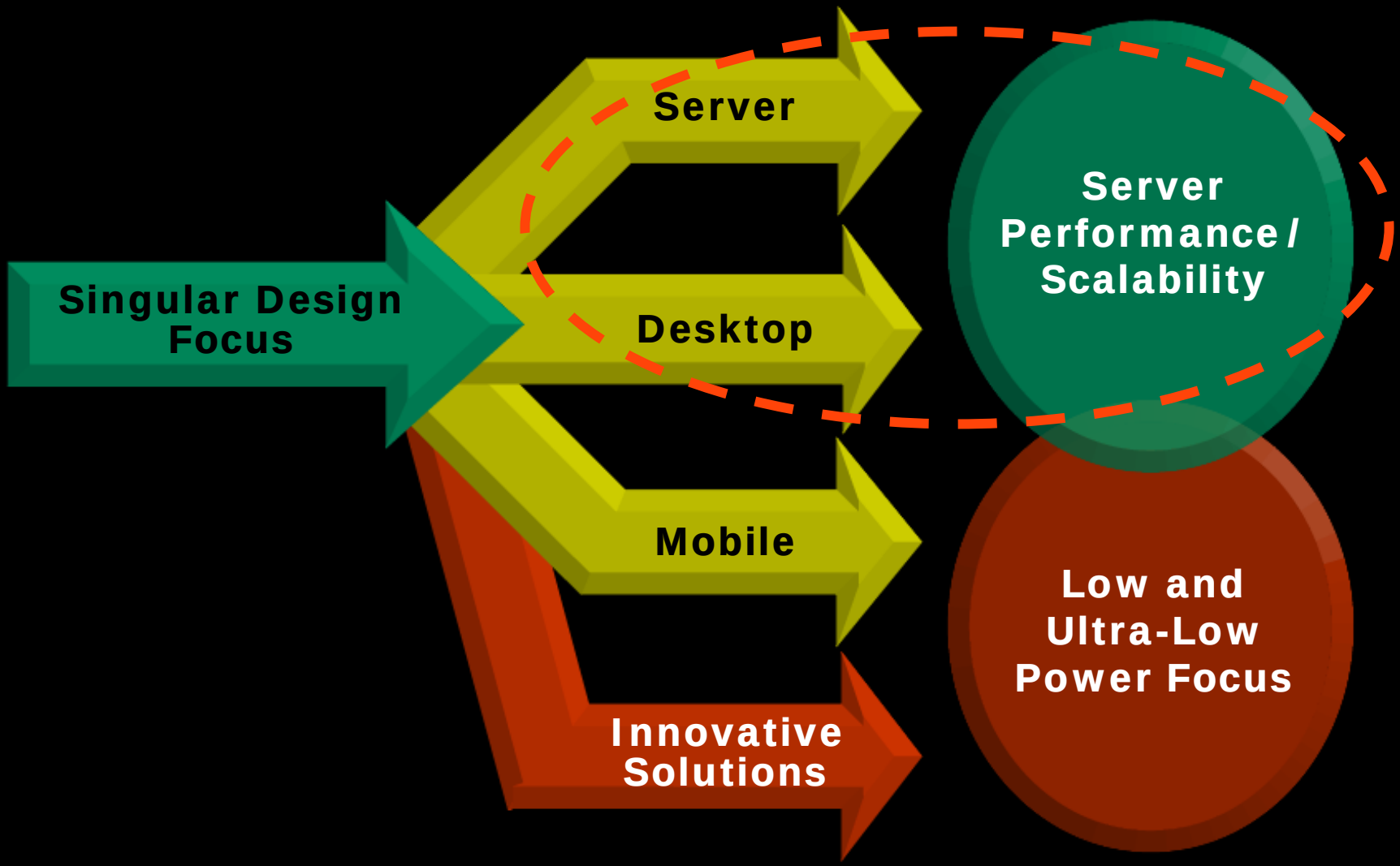
AMD

Tom Barton

Chief Executive Officer

Rackable Systems

Diversifying Design Directions to Better Serve Customers and End-Users



Enabling Faster Time to Market, Greater System Stability

Performance / power is critical — but so is differentiation, stability and speed to market

Processor

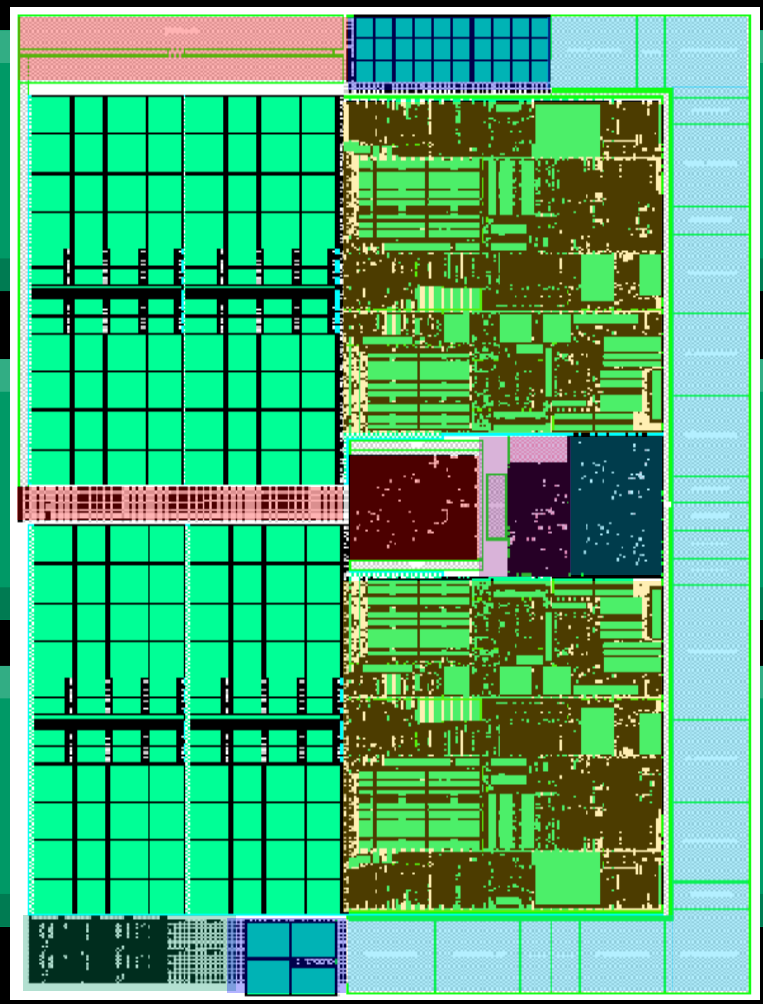
Chipset

Wireless

Integrated platform of validated technologies

Power Efficiency Improvements in AMD's New Mobile Core

- Split power planes between cores and on-die Northbridge
- Mobile-optimized on-die Northbridge
- HyperTransport 3 with link power management

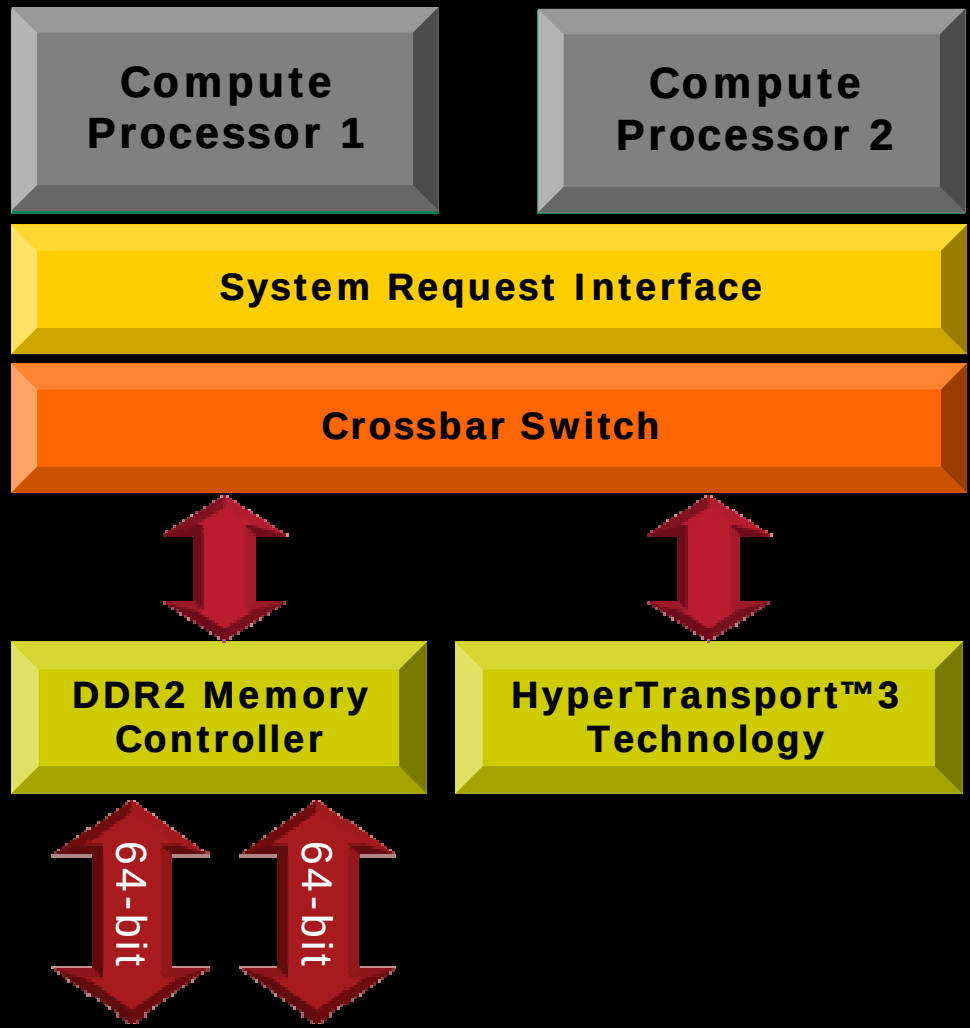


A Closer Look at Power Efficiency Improvements in New Design

Both cores can be stopped/started based on application need

HyperTransport throughput dynamically throttles based on core states

Two technologies work in concert to extend battery life



Executing in Mobile: Growing Functionality, Power Efficiency, Plus Rock-Solid Stability

2005	2006	2007
AMD Turion 64 First 64-Bit Single-Core	**AMD Turion 64 X2** First 64-Bit Dual-Core	**New Core** Mobile-Optimized & Power Managed
Increasing graphics/video features and capabilities		
DX9 UMA	Vista Aero Ready UMA	HD Video Hardware Acceleration
Increasing wireless throughput and range		
802.11 a/b/g	Draft 802.11n	802.11n/3G

Technologies Roadmap: Server and Workstation

	2006	2007	2008
Processor 	Dual-core AMD Virtualization Security Memory RAS DDR2	Next-generation Core Quad-core L3 Cache HyperTransport™ 3.0 Power Management Enhancements 128-bit FPU Increased IPC	Direct Connect Architecture 2.0 Larger Cache Manageability Virtualization+ Enhanced RAS FBDIMM
Chipset and Platform	PCI Express Gigabit Ethernet TCP Offload Serial SCSI Serial ATA II Hardware RAID	HyperTransport 3.0 PCI Express Gigabit Ethernet TCP Offload Serial SCSI Serial ATA II Hardware RAID	I/O Virtualization PCI Express 2 10 Gigabit Ethernet TCP Offload Serial SCSI Serial ATA II Hardware RAID

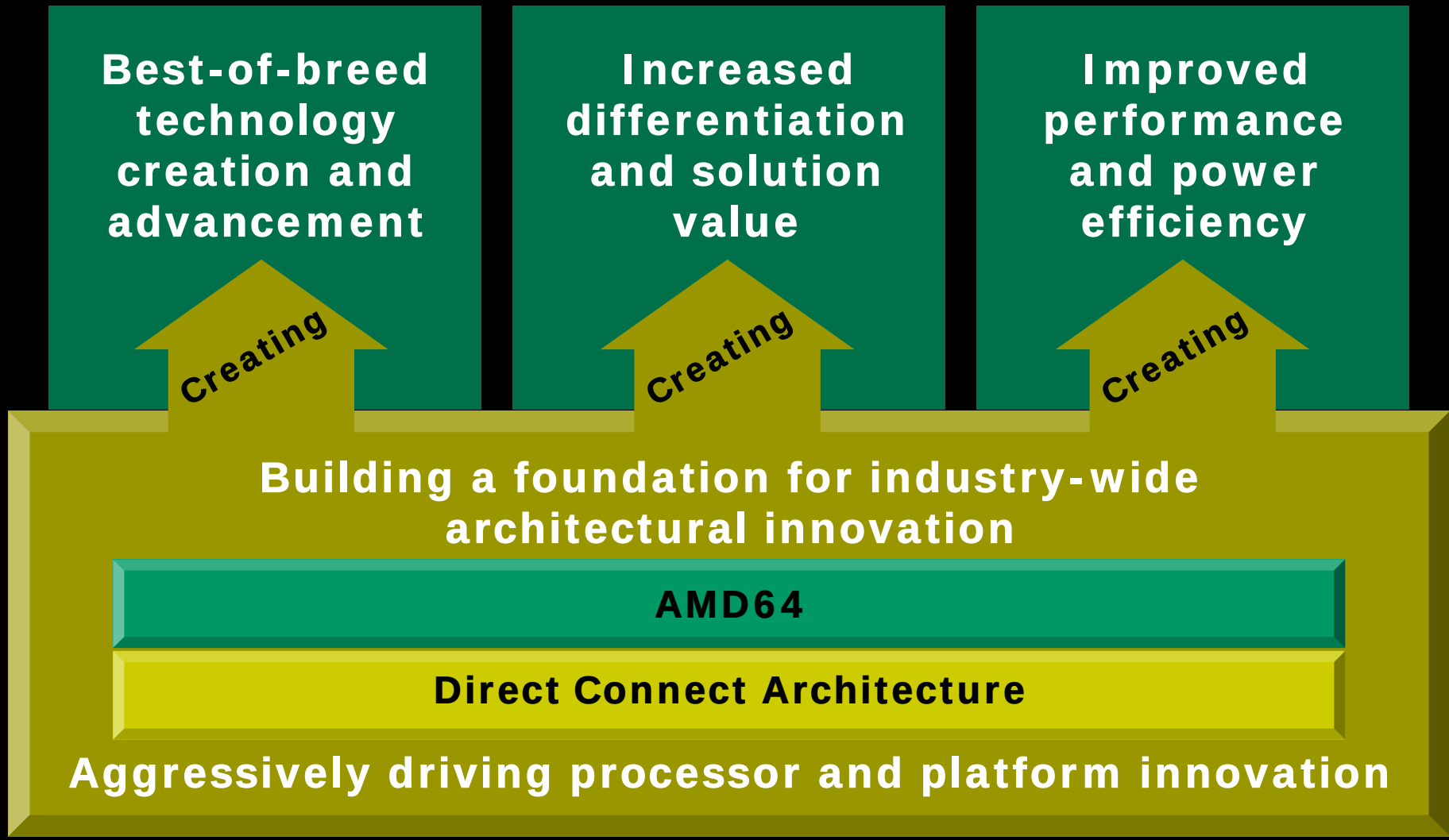
Technologies Roadmap: Desktop

	2006	2007	2008
Processors	AMD Virtualization and Security, DDR2 Energy Efficient 90nm → 65nm	Next-generation Core Larger Caches HyperTransport™ 3.0	Core Update Larger Caches HyperTransport 3.0
Performance	4x4 Dual-processor Dual-core Multi-card Graphics	4x4+ Dual-processor Quad-core Multi-card Graphics	4x4++ Dual-processor Quad-core, DDR3 Multi-card Graphics
	Dual-core, DDR2 AMD Virtualization and Security Vista® capable	Quad-core HyperTransport 3.0 Vista® ready	Quad-core, DDR3 HyperTransport 3.0 PCIe Gen II
Mainstream		Dual-core HyperTransport 3.0 Vista® ready	Dual-core, DDR3 HyperTransport 3.0 PCIe Gen II
Stable Platform	CSIP Managed Platform		
Blade PCs, Thin Clients Small Form Factor	Energy Efficient DDR2 AMD Virtualization and Security	HyperTransport 3.0	HyperTransport 3.0 DDR3

Technologies Roadmap: Mobile

	2006	2007	2008
Processors 	64-Bit Dual-core DDR2 AMD Virtualization Multi-Core Power Mgmt Digital Media Xpress	65nm New Core HT3 Link Power Mgmt Split Power Planes LV and ULV	45nm Next-generation Core DDR3
Chipsets and Platform	Vista Aero Ready UMA SATA2/AHCI HD Audio HD-DVD & Blu-Ray Draft 802.11n	HDMI HD video hardware acceleration WWAN 802.11n/3G Hybrid disk drives	Next-generation graphics Next-generation wireless connectivity

Extending the Benefits of Direct Connect Architecture

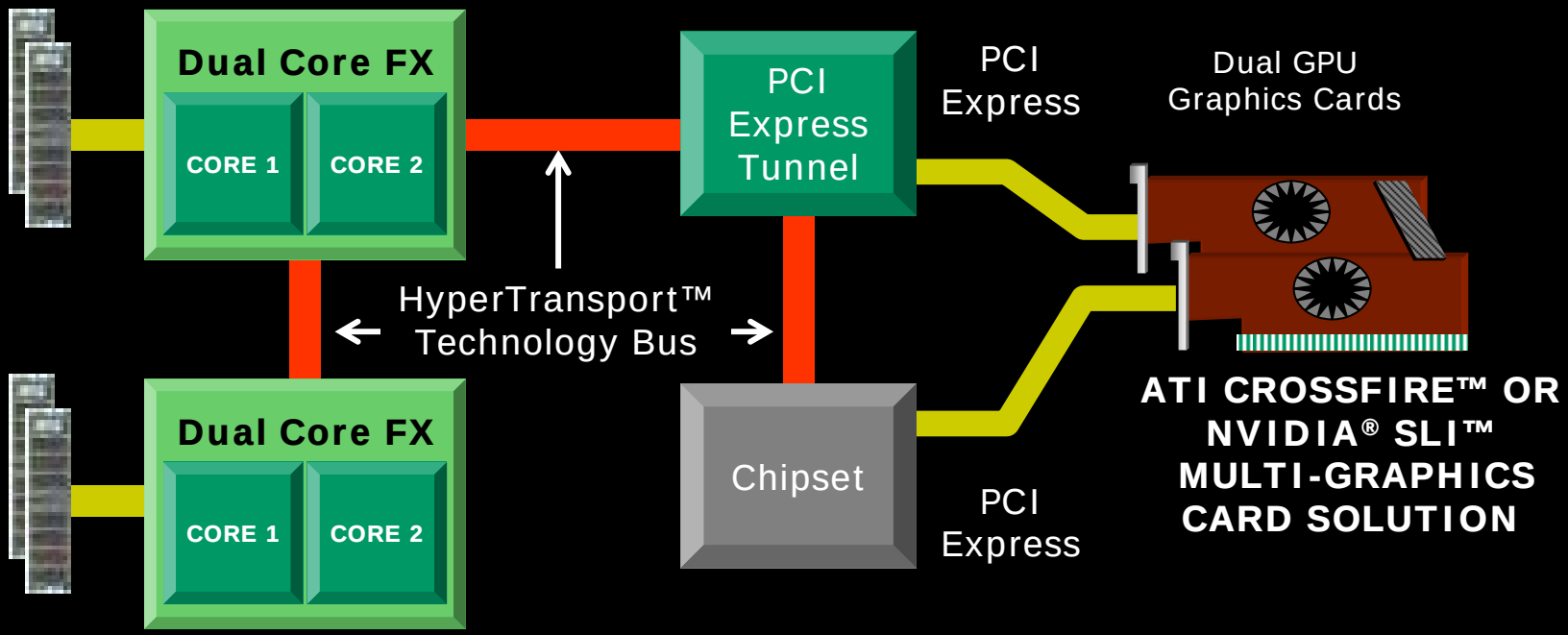


Take the Muscle Car of Gaming Add a Blower, Nitro and Pipes and What do You Get?

Announcing Today: “4x4” Enthusiasts Platform

Fully leveraging the unique benefits of Direct Connect Architecture

Extending our legendary gaming and enthusiast platform performance



It's a Multi-core and Multi-socket Future

- Enthusiasts toggle simultaneously between high-end creation and gaming
- Enthusiasts typically run an average of 7-8 applications at one time
- Digital media applications are multi-threaded
- Console development is accelerating multi-core coding
- Multi-threaded games at a tipping point with over 20 PC games in development

AMD

Nelson Gonzales
Chief Executive Officer

Alienware

Diversity of Workloads and Opportunities for Specialized Processors

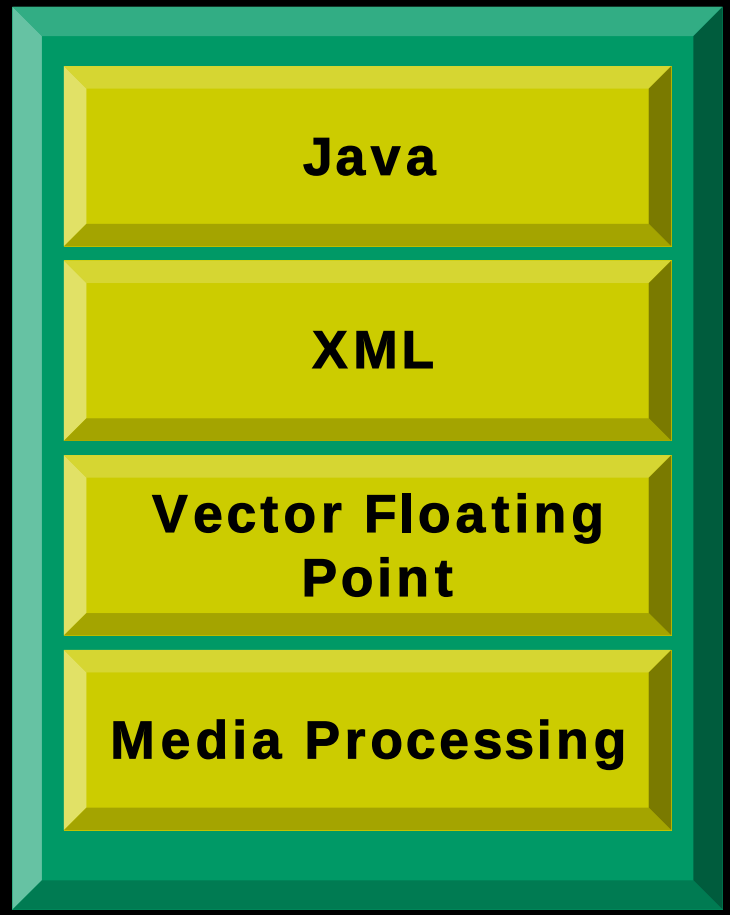
Excellent way to get power-efficient performance boosts

- Special-purpose, tuned solutions for common functions
- Drop to low-power states when not in use
- Enabled by Modern API's

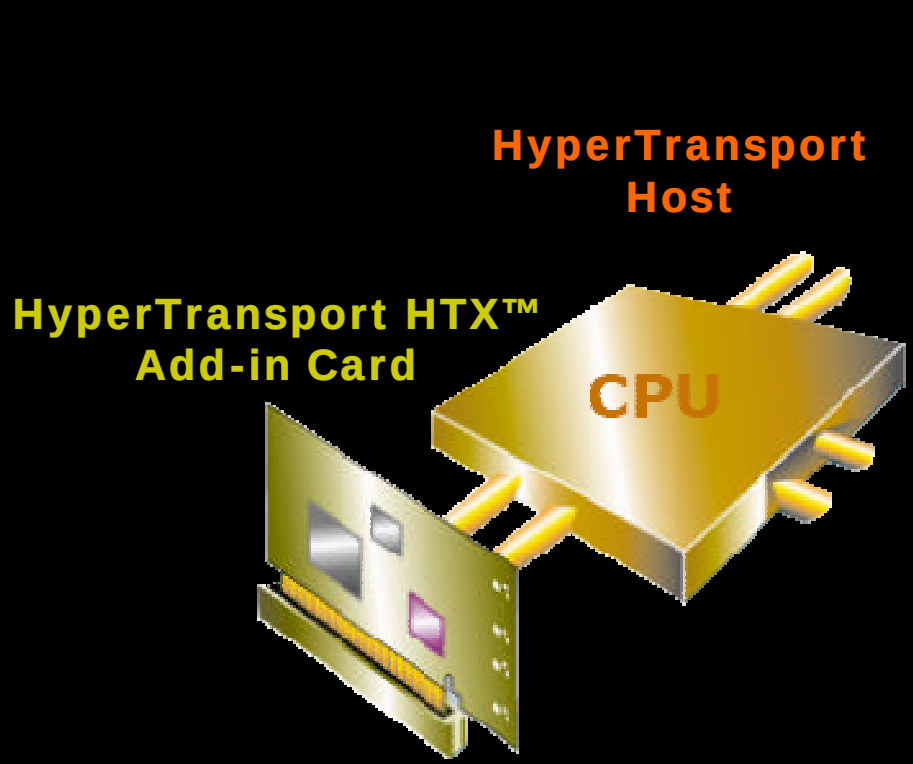
Aligns with modularity imperative

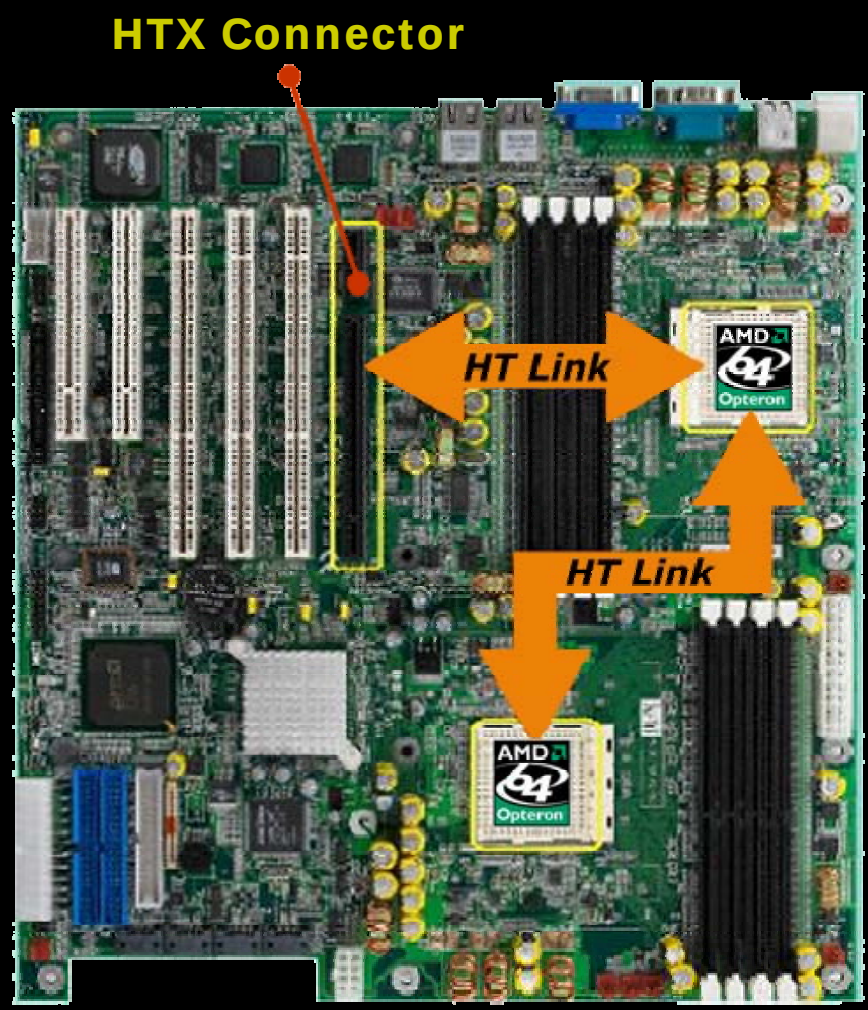
- Co-processor becomes another (optional) "IP block"
- Micro-architecture: Command delivery, Synchronization, Streaming

Many possible opportunities now, and in the future

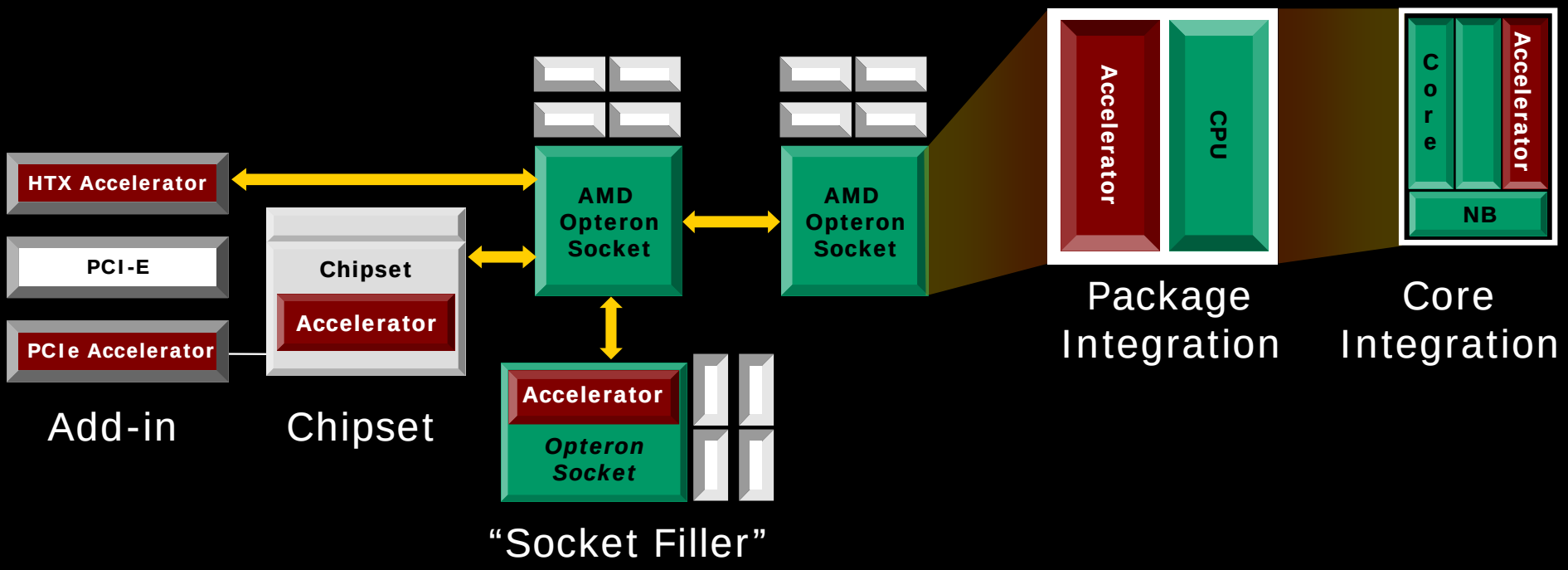


Today: HyperTransport HTX™ Enables First-Generation System-level Co-processing





Coming Soon: “Torrenza”



Increasing performance

“The Next Billion Customers”

- Rapidly diversifying needs and priorities
- Regionally-specific user trends
- Application-specific performance
- Highly tailored end-solutions
- The end of “one size fits all” computing

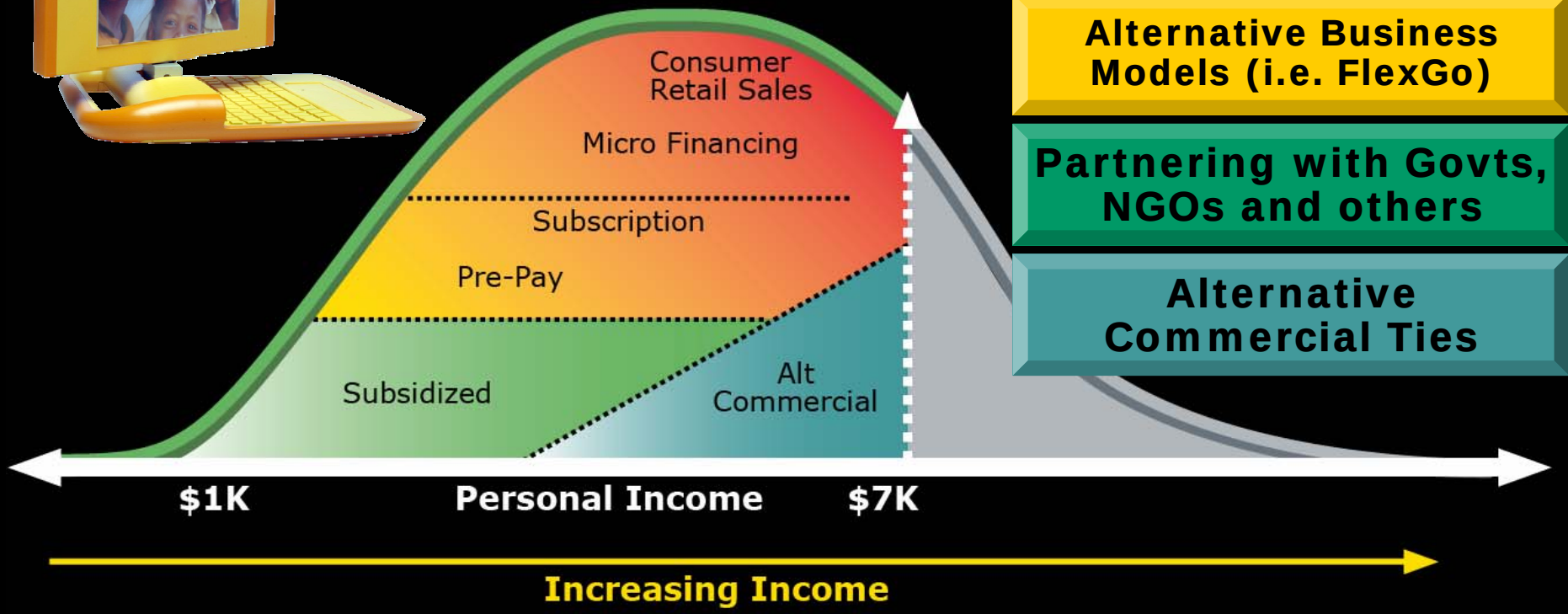







AMD

A Variety of Different Approaches and Solutions Will Be Required



New Device Categories

Alternative Business Models (i.e. FlexGo)

Partnering with Govts, NGOs and others

Alternative Commercial Ties

Architectural Leadership for Maximum Customer Benefit

Fully leveraging AMD64 and Direct Connect Architecture

Next-generation server and desktop architecture

New mobile core with optimized power management

Opening up Direct Connect Architecture

AMD64: The innovation platform.


AMD
Smarter Choice

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